REMARKS

Claims 1-4, as amended, remain herein.

Applicants appreciate the statements in the Office Action that claims 2 and 4 are allowed.

Claim 1 has been amended additionally to recite that N+1-th data is being processed in the arithmetic decision step while N-th data is being processed in the arithmetic control step; claim 3 has been amended to recite corresponding structure wording. See the Office Action mailed December 22, 2004, page 2, section 6, discussing applicants' "computing and deciding in parallel" and what was and what was not recited in the claims. Also, see applicants' Fig. 2 and description in the specification at page 19, last paragraph to page 22, second paragraph.

1. Claims 1 and 3 were rejected under 35 U.S.C. §103(a) over Chow et al. U.S. Patent 5,617,486 in view of Vassiliadis et al. U.S. Patent 4,924,422. As explained below, the claims patentably define thereover.

The Office Action mailed June 9, 2004 (upon which the

Examiner relies) describes Chow '486 as disclosing a vector processing system including a decision step for computing whether an arithmetic operation is to be performed when target data is obtained, including an arithmetic control to execute vector arithmetic and output a result. The Examiner admits that Chow '486 does not disclose performing the computing and decision steps in parallel, and cites Vassiliadis '422 as allegedly teaching same.

It was further alleged that it becomes possible to perform "calculation and decision" in parallel if the method of vector arithmetic disclosed in Chow '486 is improved by using the method taught by Vassiliadis '422. The references do not teach the invention of claims 1 and 3.

The claimed method includes an arithmetic decision step of computing and deciding whether an arithmetic process is to be executed in parallel with obtaining an arithmetic processing target data, and an arithmetic control step of exerting arithmetic control to execute the arithmetic process for the arithmetic processing target data and output a result of the arithmetic process or output the target data without executing

the arithmetic, according to a decided result in the arithmetic decision step, wherein N+1-th data is being processed in said arithmetic decision step while N-th data is being processed in said arithmetic control step. Thus, the invention enables performing vector arithmetic processing in a conditional arithmetic process. Therefore, conditional arithmetic can be divided into a process including (1) deciding whether the arithmetic should be performed or not and (2) controlling whether the arithmetic is to be executed or not according to the decided result, followed by outputting (3) a result of the arithmetic process or (4) the originally inputted data itself without executing the arithmetic process. High speed vector arithmetic can be computed because the flow of a pipeline is not interrupted by performing these processings in parallel.

Vassiliadis '422 does not teach a decision step of computing and deciding whether an arithmetic process is to be executed in parallel with obtaining an arithmetic processing target data, and an arithmetic control step of exerting arithmetic control to execute the arithmetic process for the arithmetic processing target data and output a result of the

arithmetic process or output the target data without executing the arithmetic, according to a decided result in the arithmetic decision step, wherein N+1-th data is being processed in said arithmetic decision step while N-th data is being processed in said arithmetic control step, as recited in applicants' claim 1; see corresponding wording in claim 3.

All claims 1-4 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1-4 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

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